## What is claimed is:

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

1718

19

22

23

24

25

26

27

28

29

30

- 1. A method of preventing a deadlock in a distributed shared memory system comprising a memory access request transaction queue including a plurality of queue slots, the method comprising:
- reserving one or more queue slots for exclusive processing of processor return flow control class transactions.
- 2. The method of preventing a deadlock in accordance with claim 1, further comprising:
  - allowing a processor return flow control class transaction to be processed in the reserved one or more queue slots.
  - 3. The method of preventing a deadlock in accordance with claim 2, further comprising:
  - providing a blocking flow control class transaction threshold indicating a maximum number of blocking flow control class transactions allowed to be processed in the memory access request transaction queue; and
  - preventing the memory access request transaction queue from accepting any new blocking flow control class transaction if a current number of blocking flow control class transactions already in the memory access request transaction queue is not less than the blocking flow control class transaction threshold.
- 4. The method of preventing a deadlock in accordance with claim 3, further comprising:
  - providing an entry threshold indicating a maximum number of entries allowed to be processed in the memory access request transaction queue; and
  - preventing the memory access request transaction queue from accepting any new entry if a current number of entries already in the memory access request transaction queue is not less than the entry threshold.
    - 5. The method of preventing a deadlock in accordance with claim 4, wherein:
  - each of the entry threshold and the blocking flow control class transaction threshold is configurable by at least one of a user of the distributed shared memory system and a system software; and
- wherein the entry threshold and the blocking flow control class transaction threshold are each selected so that the blocking flow control class transaction threshold is less than the entry threshold.

6. An apparatus for preventing a deadlock in a distributed shared memory system comprising a memory access request transaction queue including a plurality of queue slots, the apparatus comprising:

a coherency controller configured to reserve one or more queue slots for exclusive processing of processor return flow control class transactions.

- 7. The apparatus for preventing a deadlock according to claim 6, wherein:
- the coherency controller is configured allow a processor return flow control class transaction to be processed in the reserved one or more queue slots.
- **8.** The apparatus for preventing a deadlock according to claim 7, further comprising:
  - a first register configured to store a blocking flow control class transaction threshold indicating a maximum number of blocking flow control class transactions allowed to be processed in the memory access request transaction queue; and

wherein the coherency controller is configured to prevent the memory access request transaction queue from accepting any new blocking flow control class transaction if a current number of blocking flow control class transactions already in the memory access request transaction queue is not less than the blocking flow control class transaction threshold.

- 9. The apparatus for preventing a deadlock according to claim 8, further comprising:
- a second register configured to store an entry threshold indicating a maximum number of entries allowed to be processed in the memory access request transaction queue; and

wherein the coherency controller is configured to prevent the memory access request transaction queue from accepting any new entry if a current number of entries already in the memory access request transaction queue is not less than the entry threshold.

10. The apparatus for preventing a deadlock according to claim 9, wherein:

each of the entry threshold and the blocking flow control class transaction threshold is configurable by at least one of a user of the distributed shared memory system and a system software; and

wherein the entry threshold and the blocking flow control class transaction threshold are each selected so that the blocking flow control class transaction threshold is less than the entry threshold.